Bandwidth Efficient Baseband Multi-Modulator

Wai Fong[1], Andrew Gray[2] and Pen-Shu Yeh[1]
[1]Code 567, Goddard Space Flight Center, Greenbelt, MD 20771
[2]Jet Propulsion Laboratories, Pasadena, CA 95616

***Abstract*-The High Rate Baseband Multi-Modulator (HRBM) ASIC is being developed to provide High-Speed Bandwidth Efficient Modulations to NASA missions. Bandwidth efficiencies from 2.0 bits/symbol/Hz to 2.75 bits/symbol/Hz are selectable from three CCSDS modulations: Gaussian Minimum Shift Keying (GMSK), Filter Offset Quadrature Phase Shift Keying (Filtered-OQSK) and 8-Phase Shift Keying Trellis Coded Modulation (8-PSK TCM). An FPGA version of the HRBM is developed first to verify the individual modulation designs and characterize timing and performance issues involved with digital baseband modulation synthesis.**

A Finite Input Response (FIR) filter is included to provided baseband pulse shaping to reduce out-of-band spectral emissions. This is filter is programmable and can be tailored to meet system requirements. The ASIC is targeted to provide up to 600 Mbps throughput and will provide serial as well as parallel input. This paper provides an overview of the technology development and current status.

I. Introduction

Confronted with increasing over utilization of radio frequency (RF) spectrum, the Space Frequency Coordination Group (SFCG) imposed a spectral mask (Recommendation 21-2 [1]) for missions operating in the S- and X-bands. It's goal is to prevent adjacent inadvertent RF interference and to promote efficient spectral use of the RF spectrum. Armed with this mandate, the CCSDS panel 1E group, RF and Modulation Systems, developed a set of recommendations (2.4.17A, 2.4.17B, and 2.4.18 [2]) consistent with the SFCG mask for bandwidth efficiency. These modulation techniques range from Quadrature Phase Shift Keying (QPSK)-type modulations, i.e. GMSK, Filtered-OQPSK, Shaped-OQPSK (S-OQPSK), Feher QPSK-Type B (FQPSK-B) and also higher-order coded modulations, i.e. 8-PSK TCM at 2.0, 2.25, 2.5, and 2.75 bits/symbol/Hz (a general reference for the principles of these modulations can be found in [4], and for performance and implementation information look in [3, 6]).

The main concept behind the selection of the CCSDS modulations is the idea of pulse shaping the modulated waveform to reduce sideband emissions. There are two methods for pulse shaping the modulated waveform: 1. RF filtering after the transmitter power amplifier or 2. baseband filtering prior to RF modulation before the power amplifier. The HRBM utilizes the latter approach with the advantage that the pulse shaping can be digitally synthesized with finite impulse response (FIR) filtering. This allows for flexibility as practically any filter design can be implemented by reprogramming the tap coefficients of the FIR.

The HRBM is developed to allow digital synthesis of a subset of the CCSDS modulation schemes as well as the inclusion of other non-CCSDS schemes (i.e. 8-PSK, 16-QAM, and BPSK) that could be used in other frequency bands.

II. Modulation Selection

CCSDS recommendation 2.4.17A [2] specifies four base Offset Quadrature Phase Shift Keying (OQPSK) type modulations. GMSK, Filtered-OQPSK, Shaped-Offset Quadrature Phase Shift Keying (S-OQPSK), Feher Quadrature Phase Shift Keying (FQPSK). Although each modulation are unique in power spectral density (PSD) response, they all conform to the requirements of the SFCG mask. Figs. 1, 2, and 3 show computer generated PSD responses for the GMSK, Filtered QPSK and 8-PSK TCM modulations. Note that all of the responses fall below the mask. Also notice that there are in effect two masks, one for symbol rates (SR) below 2 Mbps and another for rates above 2 Mbps. From the group of four CCSDS rec. 2.4.17A modulations, two modulations were selected: GMSK and Filtered-OQPSK. Recommendation 2.4.18 which specifies 8PSK-TCM in four spectral efficiencies: 2.0, 2.25, 2.5 and 2.75 bits/symbol/Hz are also included. Although 8PSK-TCM modulations are not constant envelop modulations, they can be filtered to conform to the mask as Fig. 3 shows.

A. GMSK for BT_S=0.25 and 0.5

The rationale for selecting GMSK is based on a number of considerations. First, in terms of side band suppression, BT_s=0.25[a], (where B is the bandwidth of the Gaussian filter and T_s is the bit period) GMSK gives one of the best performance of all modulations. The floor of the mask starts at -60 dB when $-3 > f/R_s > 3$. Fig. 1 clearly shows no sign of signal strength at these frequency ranges. In fact, the PSD will fall below -90 dB when $-1.5 > f/R_s > 1.5$ well within the mask. And the PSD is well below 20 dB of the mask for any point $-0.5 > f/R_s > 0.5$. For BT_s=0.5, it's PSD is broader than BT_s=0.25 but still within the mask. The PSD will fall below -90 dB when $-2.3 > f/R_s > 2.3$. In terms of occupied bandwidth (defined by International Telecommunications Union as the 99% power containment bandwidth), GMSK BT_s=0.25

[a] All bit and symbol rate terminology will conform to convention used in [3].

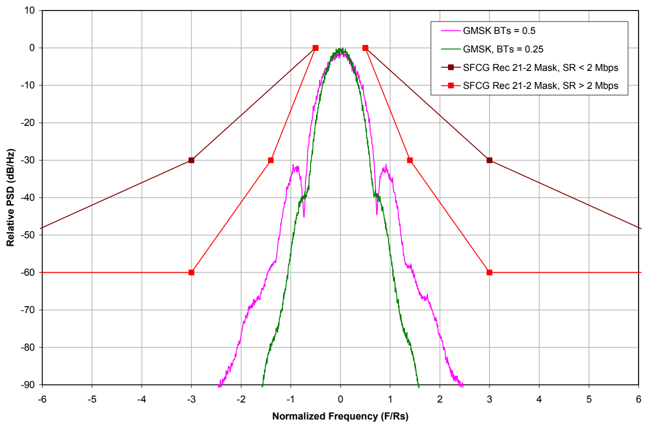

Fig. 1. The PSD of GMSK Modulations with SFCG mask

has a 0.88 R_s (normalized frequency) while GMSK BT_s=0.5 has a 1.03 R_s (normalized frequency) [3]. In regards to equipment availability, GMSK has a large commercial receiver base due it's prevalent use in European communication links. And finally, GMSK is a constant envelope modulation meaning the power amplifier of the spacecraft can operate at the 0 dB back off point with out the spectral regrowth problem.

B. Filtered OQPSK

CCSDS recommendation 2.4.17A [2] specify two filter types: square root raised cosine (SRRC) filter (with roll-off factor α = 0.5) and six-pole Butterworth filter with a BT_s=1.0 (where B is the 3-dB filter bandwidth and T_s is the bit period). In addition, the recommendation leaves open the option of using any filter that will conform to the SFCG mask. Fig. 2 shows the PSD of Filtered OQPSK with the two specified filter types. And although the waveforms are not as spectrally contained as the GMSK waveforms, they do conform to the mask. In fact, the PSDs are at least 10 dB below the SR > 2 Mbps mask and the occupied bandwidth is 0.88 R_s for both filter types [3].

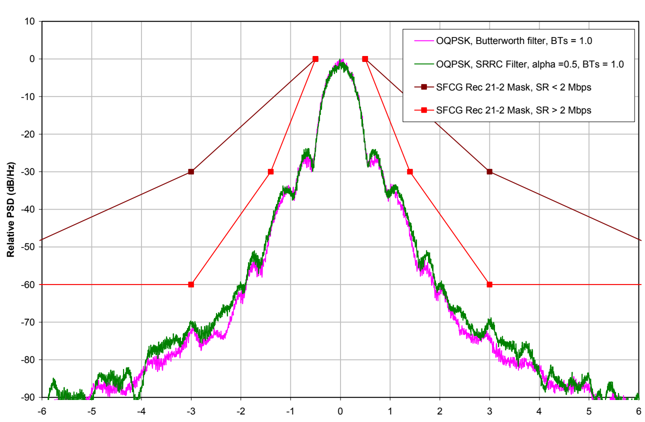

Fig. 2. The PSD of Filtered OQPSK Modulations with SFCG mask

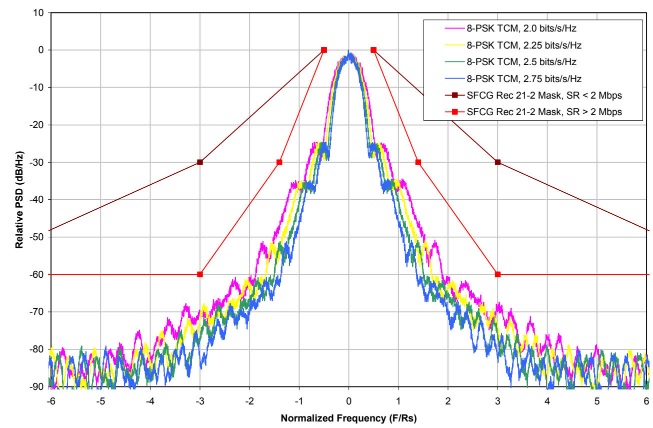

Fig. 3. The PSD of 8-PSK TCM Modulations with SFCG mask

C. 8-PSK TCM

CCSDS recommendation 2.4.18 recommends multi-dimensional trellis coded modulation on an 8-PSK signal space. This modulation is actually a combination of channel coding and modulation. It's advantages are better bit error rate (BER) performance over the uncoded 8-PSK case and built-in phase ambiguity resolution. Of course, this comes at the expense of more complexity at the receiver. As there's a requirement of a Viterbi decoder to properly demodulate the received signal. This modulation also requires filtering to conform to the SFCG mask as demonstrated in Fig. 3. Note that for a distortionless channel, the PSD is at least 10 dB below the mask. The filtering, however, will produce signal amplitude variations which when driven into a power amplifier at 0 dB back off will produce spectral regrowth and possibly violate the SFCG mask. Therefore, the power amplifier must be set to operate in the linear region, e.g. 3 dB backed off to avoid spectral regrowth.

D. Other modulations

The non-CCSDS modulations are Filtered Binary Phase Shift Keying (Filtered BPSK[b]), Filtered 8-PSK, Filtered 16-Phase Shift Keying (Filtered 16-PSK), Filtered 16 Quadrature Amplitude Modulation (Filtered 16-QAM). These modulations are added due to their very low, almost trivial, implementation costs. Note, the authors are not advocating these modulations for spacecraft use. However if other applications exist where there is a need for these types of modulations, this possibility alone would justify adding them into the HRBM.

[b] Although Filtered BPSK is not an official CCSDS RF and Modulation Systems Blue Book Recommendation [2], there are many references to unfiltered BPSK in that text.

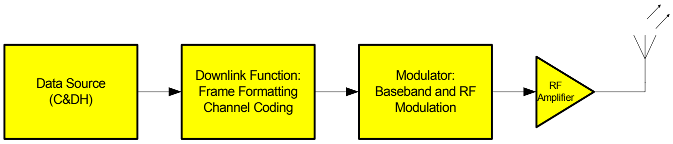

Fig. 4. Spacecraft Downlink Communication Block Diagram

II. Spacecraft Communication System

Fig. 4 is a block diagram of the spacecraft downlink communication function. The data source, which usually is comes from the command and data handling (C&DH) or a mass storage device, is presented to the downlink function block whose job is to frame format and channel encode the data. The formatted/coded data is then passed to the modulator to provide RF modulation prior to amplification and transmission.

III. HRBM description

Within the modulator, the baseband modulator is responsible for taking the formatted and/or coded digital data stream and producing baseband In-phase (I) and Quadrature (Q) analog signals (see Fig. 5). These I/Q signals are then passed to the RF modulator whose function is to phase modulate an RF carrier with the I/Q signals.

In this architecture, the baseband modulator defines the type of modulation technique used by the communications link.

III. Asic Architecture

Fig. 6 shows a diagram of the HRBM internal architecture within the block diagram of the baseband modulator. The HRBM generates discrete signals and requires two digital-to-analog converters (DAC) and smoothing filters. Note that this diagram does not include all modulations, just the major ones. Data is presented either in serial or parallel form, however in the figure, only serial is shown. Taking the serial input as an example, Bits_In_1 is the serial input data port and Clk1 is it's associated clock. Only in the case of Asynchronous Filtered OQPSK are the inputs of Bits_In_2 and Clk2 is used to allow for two independent data streams.

Clocking for the TCM-type modulations can be difficult due to the fractional bandwidth efficiencies defined by trellis encoder and constellation mapper [3].

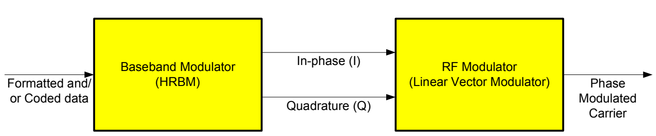

Fig. 5. Modulator Block Diagram

A. Digital Wavelet I/Q Synthesis

OQPSK-type of modulations can be generated by the use of wavelets. Typically, a waveform can be divided into 4 wavelets per single bit time. These wavelets are stored in 8-bit wide look-up tables. For every bit sequence, a corresponding wavelet sequence is produced but at a rate 4 times the input data rate. Each wavelet is presented at the output of the HRBM where these values are passed to the DAC and smoothing filters producing the entire analog waveforms. In the HRBM, the GMSK modulations are generated with this method. In general, there many ways to synthesis GMSK waveforms [6]; this method is the closest to the architecture of the Filtered OQPSK and 8-PSK TCM designs where a DAC is used as the final conversion to analog form.

B. FIR Filter

With the exception of GMSK modulations, the FIR filter plays a center role in the waveform synthesis. Fig. 6 demonstrates this point, from the inputs the data go through a serial to parallel conversion and then a multiplexing structure to provide inputs to the FIR. With TCM modulations, there is the additional simple logic encoding in between the multiplexers and the FIR. Not only does the FIR play a prominent role, it also dominates the real-estate of the FPGA or ASIC, consuming 95% of the utilized chip space.

For Filtered OQPSK there is the additional option of having asynchronous In-phase (I) and Quadrature (Q) inputs with the possibility of differential data rates on I/Q. To account for this functionality, the inclusion of separate infinite impulse filtering (IIR) is necessary to provide filtering for the lower data rate channel while the higher rate channel is filtered by the FIR.

The FIR filter is a 64 tap structure operating in the frequency domain—a feature that allows for higher data rates and less complexity (a reduction of 8 in the number of multipliers as opposed to a time domain FIR filter). Refer to Proakis and Manolakis for a good explanation on FIR filters [7]. (Note that the same FIR filter is used in the Filtered OQPSK modulation, 8-PSK- type modulations and all other filtered modulations.) A discrete Fourier transform (DFT) is used to convert the signal into the frequency domain. The filter consist of a set of 120 multipliers with dimensions of 14 bits (coefficients) by 12 bits (DFT outputs). After the filtering, an inverse discrete Fourier transform is performed to bring the frequency domain signals into the time domain. These values are then outputted to the DACs.

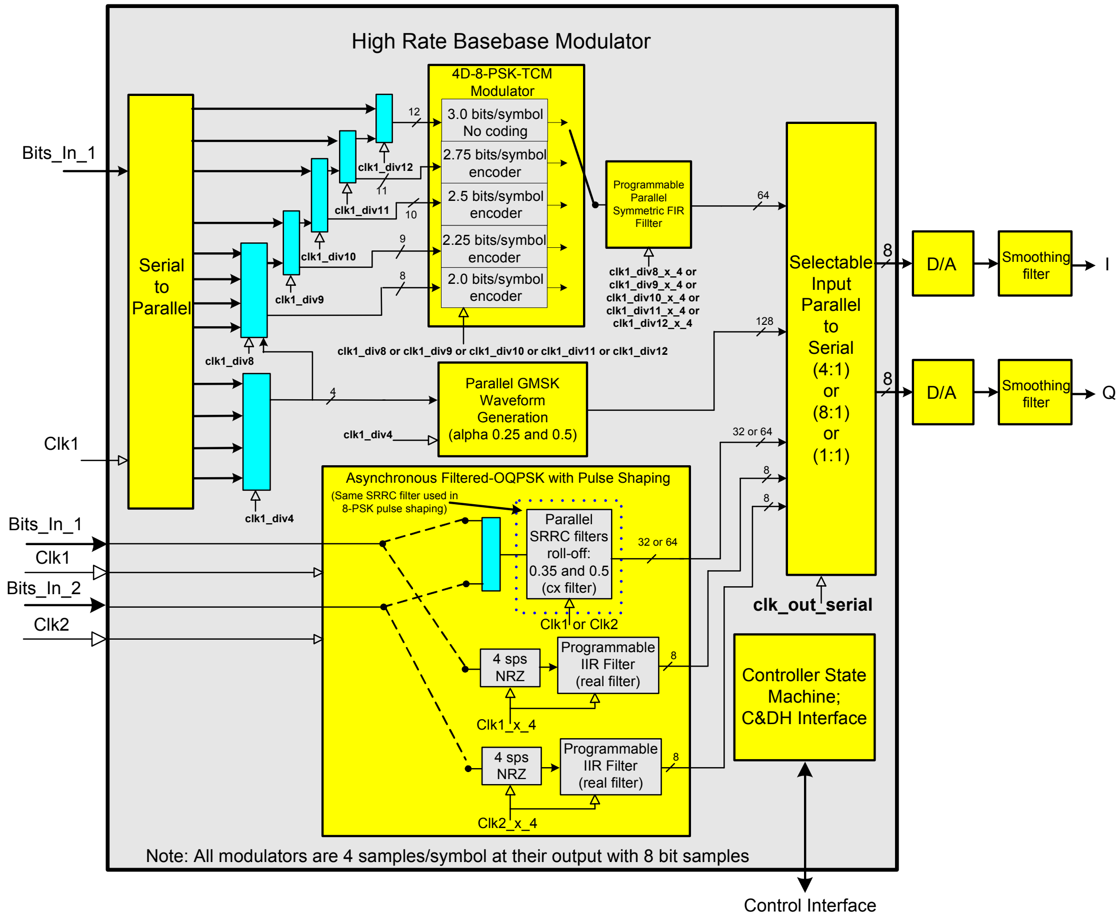

Fig. 6. Baseband Modulator Block Diagram

IV. Performance Considerations

Simulation runs indicate that 64 tap FIR filter with 8-PSK modulation will operate with low implementation loss (around 1dB) for an undistorted channel. This is only the beginning of the system simulations as channel distortions, transmitter distortions and receiver losses will be included in the study to make sure that the best design is put forth.

Since the goal of the ASIC implementation is to contain all of the modulations in one IC, a trade off in reducing the number of taps to 32 may be necessary to reduce the size of the ASIC. (Remember that a majority of the chip real estate is in the FIR alone.) Of course, any changes of this magnitude would be analyzed in detail to ensure good performance is achieved.

V. Test Scenerios

Once the FPGA version of HRBM is completed and the prototype board is checked out, the plan would be to perform a Tracking and Data Relay Satellite System (TDRSS) loop test at White Sands, NM on the new Ka-band channel service (and possibly the existing Ku-band channel service) with a linear vector modulator and power amplifier provided by the Solar Dynamics Observer (SDO) project. The White Sands test is repeated when the ASIC prototype board is built. The ASIC is targeted to operate at greater than 300 Mbps.

VI. Schedule And Status

There are two development tracks: 1. flight ASIC modulator along with the ASIC demodulator/decoder and 2. the FPGA modulator. As of the beginning of June 2003, most of the individual modulations has been designed, verified and translated into a Xilinx FPGA. The FPGA FIR filter design has been simulated to 100 MHz operation. This corresponds to an input date rate of 300 Mbps with Filtered 8-PSK. The FPGA prototype board design is complete and submitted for fabrication. By September 2003, this board should be completely checked out. In parallel, the ASIC design has started and is currently undergoing an architectural study. After this is competed, a detail design should start sometime in September 2003 and a fabrication run would be initiated by the fourth quarter 2003 with the chips delivered in the first quarter 2004.

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